CLAIMS

- 1. (Currently amended) A GaN based enhancement mode MOSFET, comprising:
- a (Group III)_xGa_{1-x}N layer, where x is from 0 to 1, disposed on said GaN layer, a

a GaN comprising layer;

- a <u>doped semiconductor</u> source and a <u>doped semiconductor</u> drain extending through said (Group III)_xGa_{1-x}N layer into said GaN layer, said source and drain separated by a channel region <u>comprising said (Group III)_xGa_{1-x}N layer and said GaN layer, wherein a first p-n junction is <u>formed where said source contacts said channel region and a second p-n junction is formed</u> where said drain contacts said channel region;</u>
 - a gate dielectric layer disposed over said channel region, and

thickness of said (Group III)_xGa_{1-x}N layer being less than 20 nm;

- a gate electrode <u>overlapping said source and said drain</u> disposed on said gate dielectric, wherein said MOSFET is in an off-state when said gate is not biased.
 - 2. (Original) The transistor of claim 1, wherein said Group III element comprises Al.
 - 3. (Original) The transistor of claim 1, wherein x is from 0.2 to 0.35.
 - 4. (Original) The transistor of claim 1, wherein said Group III element comprises B.
 - 5. (Original) The transistor of claim 1, wherein MOSFET is an n-channel MOSFET.

- 6. (Original) The transistor of claim 1, wherein MOSFET is a p-channel MOSFET.
- 7. (Original) The transistor of claim 1, wherein said (Group III)_xGa_{1-x}N layer is undoped.
 - 8. (Original) The transistor of claim 1, wherein said (Group III)_xGa_{1-x}N layer is p-doped.
- 9. (Original) The transistor of claim 1, wherein said thickness of said (Group III)_xGa_{1-x}N layer is less than 10 nm thick.
- 10. (Original) The transistor of claim 1, wherein said thickness of said (Group III)_xGa_{1-x}N layer is less than 5 nm thick.
- 11. (Original) The transistor of claim 1, wherein said thickness of said (Group III)_xGa_{1-x}N layer is 1 to 4 nm thick.
- 12. (Original) The transistor of claim 1, wherein said GaN comprising layer is selected from the group consisting of p-GaN, undoped GaN and InGaN.
- 13. (Original) The transistor of claim 1, further comprising a p-AlGaN or undoped AlGaN layer disposed below said GaN comprising layer.

- 14. (Currently amended) The transistor of claim 1, wherein said gate dielectric layer comprises SiN_x [[, MgO or Sc₂O₃]].
 - 15. (New) The transistor of claim 1, wherein said gate dielectric layer comprises MgO.
 - 16. (New) The transistor of claim 1, wherein said gate dielectric layer comprises Sc_2O_3 .